IN THE SPECIFICATION

Please amend the paragraphs of the specification as follows:

[0001] The present Application for Patent is a Continuation and claims priority to Patent Application No. 09/182,367 entitled "Method And Apparatus For Multipath Demodulation In A Code Division Multiple Access communication System," filed October 27, 1998, now ~~allowed~~ U.S. Patent No. 6,625,197, and assigned to the assignee hereof.

[0039] The frequency error estimates from each finger **44a-c** are combined and integrated in frequency error combiner **26**. The integrator output, LO_ADJ **36**, is then fed to the voltage control of the TCXO in the analog transmitter and receiver 16 to adjust the clock frequency of the CHIPX8 clock **40**, thus providing a closed loop mechanism for compensating for the frequency error of the local oscillator. Fingers 12a-c are coupled to power combiner 24 which outputs a transmit gain signal 38 to analog transmit and receiver 16.

[0062] Searcher **114** reports the energies in a window around peaks **50**, **54** and **58**. Microprocessor **130** determine from the reported energies that peaks **50** and **58** were narrow and could be successfully demodulated with a single path demodulator. Microprocessor **130** would also be able to identify the multipath component at peak **54** as a fat path and would assign for its demodulation the fat path demodulator of the present invention. So for example, fingers **112a** and **112b** demodulate single paths and are assigned to paths **50** and **58** of FIG. 3. Finger **112c**, on the other hand, are directed by microprocessor **130** to perform a fat path demodulation and would be assigned to demodulate path **54**. Fingers **112a-c** are coupled to both symbol combiner **122** and frequency error combiner **126**. Symbol combiner **122** outputs a symbol data 146 to deinterleaver decoder **128** and frequency error combiner **126** outputs a LO_ADJ **136** to analog transmit and receiver **116**.

[0063] FIG. 5 illustrates a novel RAKE receiver structure that uses a single accumulator instead of an accumulator for each finger as is provided in current RAKE receiver structures.

The digitized samples are provided to complex PN despreader **150** of demodulator **158**. In the exemplary embodiment, the signals are complex PN spread as described in U.S. Patent Application Serial No. 08/856,428, entitled "HIGH DATA RATE CDMA WIRELESS CMMUNICATION SYSTEM USING VARIABLE SIZED CHANNEL CODES," filed May 14, 1997, now abandoned, assigned to the assignee of the present invention, in accordance with the following equations:

$$I = I' PN_I + Q' PN_Q \quad (4)$$

$$Q = I' PN_Q - Q' PN_I. \quad (5)$$

where PN_I and PN_Q are distinct PN spreading codes and I' and Q' are two channels being spread at the transmitter. Complex PN despreader **150** removes the complex spreading based on the PN codes, PN_I and PN_Q, to provide two complex PN despread signals.

[0080] After one half PN chip interval, switch **202** toggles so as to put the next sample, received one half PN chip interval later, on input line **199** to demodulators **200b** and **200d.** Within demodulator **200b**, the sample is PN descrambled in PN descrambling element **204b**. As described previously PN descrambling element **204b** descrambles the sample in accordance with two PN sequences (PN_I and PN_Q) provided by PN generator **[[206b]] 206**. The PN sequences are delayed by delay element **208** by one PN chip period.

[0084] The complex PN descrambled sequences are provided to a first input of complex conjugate multiplier **212d** and to pilot filter **210d**. Pilot filter **[[210c]] 210d** uncovers the pilot channel in accordance with the Walsh covering for the pilot channel W_{pilot}. In the exemplary embodiment, pilot filter **210d** is simply a low pass filter that removes the noise from the pilot signal. The complex conjugate of the filtered pilot signal and the complex PN despread sequences are multiplied in complex conjugate multiplier **212d** which computes the dot product of the pilot channel conjugate and the PN descrambled sequence to provide a scalar sequence to Walsh sequence multiplier **214d**.

[0087] In FIG. 7, a second fat path demodulator is illustrated where the delays are applied to the input signal instead of the demodulation elements. In FIG. 7, four demodulators **300a-300d** are provided to demodulate paths that are a fixed half PN chip distance from one another. The demodulators move together demodulating PN offsets that are offset from one another by fixed increments. As described previously a microprocessor could be used to vary the amount of delay provided by delay elements **320** and **322**. In the exemplary embodiment, one of the demodulators is the master and tracks the peak of set of multipath signals and the other demodulators act as slaves and follow the master demodulator. In the exemplary embodiment, a metric such as the power from pilot filter **[[210]] 310** can be used by the master finger to track the movement of the peak.

[0090] The first sample is provided through switch **302** on line **298** to demodulator **300a.** The sample is PN descrambled in PN descrambling element **304a**. In the exemplary embodiment, PN descrambling element **[[204a]] 304a** descrambles the sample in accordance with two PN sequences (PN_I and PN_Q) provided by PN generator **[[206]] 306**. The complex despreading operation is performed as described above with respect to complex despreading element **[[150a]] 150.**

[0091] The complex PN descrambled sequences are provided to a first input of complex conjugate multiplier **312a** and to pilot filter **310a**. Complex conjugate multiplier removes phase ambiguities that are introduced by the propagation path. Pilot filter **310a** uncovers the pilot channel in accordance with the Walsh covering for the pilot channel W_{pilot}. In the exemplary embodiment, W_{pilot} is the all zeroes Walsh sequence for which the uncovering operation is a No Op. In this special case, pilot filter **310a** is simply a low pass filter which removes the noise from the pilot signal. The complex conjugate of the filtered pilot signal and the complex PN despread sequences are multiplied in complex conjugate multiplier **312a** which computes the dot product of the pilot channel conjugate and the PN descrambled sequence to provide a scalar sequence to Walsh sequence ~~multiplier**314a**~~ multiplier **314a.**

[0092] Walsh sequence multiplier **314a** multiplies the input scalar sequence from complex conjugate multiplier **312a** by the Walsh traffic sequence from Walsh generator **318**. The multiplied sequence is then provided to combiner element **[[224]] 324.**

[0094] The complex PN descrambled sequences are provided to a first input of complex conjugate multiplier **312c** and to pilot filter **310c**. Pilot filter **310c** uncovers the pilot channel in accordance with the Walsh covering for the pilot channel W_{pilot}. In the exemplary embodiment, W_{pilot} is the all zeroes Walsh sequence for which the uncovering operation is a No Op. In this special case, pilot filter **310c** is simply a low pass filter which removes the noise from the pilot signal. The complex conjugate of the filtered pilot signal and the complex PN despread sequences are multiplied in complex conjugate multiplier **[[212c]] 312c** which computes the dot product of the pilot channel conjugate and the PN descrambled sequence to provide a scalar sequence to Walsh sequence multiplier **[[214c]] 314c.**

[0096] After one half PN chip interval, switch **302** toggles so as to put the next sample, received one half PN chip interval later, on input line **299** to demodulators **300b** and **300d.** Within demodulator **300b**, the sample is PN descrambled in PN descrambling element **304b**. In the exemplary embodiment, PN descrambling element **304b** descrambles the sample in accordance with two PN sequences (PN_I and PN_Q) provided by PN generator **[[306b]] 306.**

[00104] The first sample is provided through switch **402** onto line **[[398]] 318** to demodulator **400a.** The sample is PN descrambled in PN descrambling element **404a**. In the exemplary embodiment, PN descrambling element **404a** descrambles the sample in accordance with two PN sequences (PN_I and PN_Q) provided by PN generator **406** as described previously.

[00107] The first sample is redundantly provided through switch **402** on line **[398] 318** to delay element **[[420]] 422a**. Delay element **[[420]] 422a** delays the signal by one PN chip interval prior to providing the sample to demodulator **400c.** Thus, the signal successfully demodulated by demodulator **400c** will have traversed a propagation path that required one PN chip less time to traverse than the path that was successfully demodulated by demodulator **400a**. The sample is PN descrambled in PN descrambling element **404c**. In the exemplary embodiment, PN descrambling element **404c** descrambles the sample in accordance with two PN sequences (PN_I and PN_Q) provided by PN generator **406.**

[00113] After one half PN chip interval, switch **402** toggles so as to put the next sample, received one half PN chip interval later, on input line **[[399]] 319** to demodulators **400b**, **400d** and **400f.**

[00114] Within demodulator **400b**, the sample is PN descrambled in PN descrambling element **404b**. In the exemplary embodiment, PN descrambling element **404b** descrambles the sample in accordance with two PN sequences (PN_I and PN_Q) provided by PN generator **[[406b]] 406**. The complex PN descrambled sequences are provided to a first input of complex conjugate multiplier **412b** and to pilot filter **410b**. Pilot filter **410b** uncovers the pilot channel in accordance with the Walsh covering for the pilot channel W_{pilot}. In the exemplary embodiment, pilot filter **410b** is simply a low pass filter which removes the noise from the pilot signal. The complex conjugate of the filtered pilot signal and the complex PN despread sequences are multiplied in complex conjugate multiplier **412b** which computes the dot product of the pilot channel conjugate and the PN descrambled sequence to provide a scalar sequence to Walsh sequence multiplier **414b**.

[00116] The second sample is redundantly provided through switch **402** on line **[[399]] 319** to delay element **420a**. Delay element **420a** delays the signal by one PN chip interval prior to providing it to demodulator **400d**. Demodulator **400d** successfully demodulates a signals that traversed a path that took one PN chip less time to traverse than the path successfully demodulated by demodulator **400b.** The second sample is PN descrambled in PN descrambling element **404d**. In the exemplary embodiment, PN descrambling element **404d** descrambles the sample in accordance with two PN sequences (PN_I and PN_Q) provided by PN generator **406**.

[00140] The first sample is provided directly to demodulators **600a** and **600b** and is delayed by one PN chip interval by delay elements **620** and **622** before being provided to demodulators **600c** and **600d**, respectively. The sample is PN descrambled in PN descrambling elements **604a**, **604b**, **604c** and **604d**. In the exemplary embodiment, PN descrambling elements **604a**, **604b**, **604c** and **604d** descramble the sample in accordance with two PN sequences (PN_I and PN_Q) provided by PN generator **606**. The complex descrambling operation is performed as described above with respect to complex despreading element **[[150a]] 150**.

[00143] The second sample is, then, provided directly to demodulators **600a** and **600b** and is delayed by one PN chip interval by delay elements **620** and **622** before being provided to demodulators **600c** and **600d**, respectively. The sample is PN descrambled in PN descrambling elements **604a**, **604b**, **604c** and **604d**. In the exemplary embodiment, PN descrambling elements **604a**, **604b**, **604c** and **604d** descramble the sample in accordance with two PN sequences (PN_I

and PN_Q) provided by PN generator **606**. The complex descrambling operation is performed as described above with respect to complex despreading element **[[150a]] 150**.

[00147] FIG. 11 illustrates a modification to FIG. 10 which is applicable to all of the previous embodiments illustrated in FIGS. 6, 7, 8 and 9. FIG. 11 illustrates a modification to FIG. 10 which allows for the elimination of all but one Walsh multiplier. In ~~FIG. 10~~ FIG. 11, four demodulators **650a**, **650b**, **650c** and **650d** are provided to demodulate paths that are a fixed half PN chip distance from one another. The received samples are provided at twice the PN chip rate to demodulators **650a**, **650b**, **650c** and **650d**. Pilot filters **660a** and **660c** ignore the even samples and pilot filters **660b** and **660d** ignore the odd samples. Combiner **674** only combines demodulated odd samples from demodulators **650a** and **650c** with demodulated even samples from demodulators **650b** and **650d**.

[00148] The first sample is provided directly to demodulators **650a** and **650b** and is delayed by one PN chip interval by delay elements **670** and **672** before being provided to demodulators **650c** and **650d**, respectively. The sample is PN descrambled in PN descrambling elements **654a**, **654b**, **654c** and **654d**. In the exemplary embodiment, PN descrambling elements **654a**, **654b**, **654c** and **654d** descramble the sample in accordance with two PN sequences (PN_I and PN_Q) provided by PN generator **[[656]] 606**.

[00151] The second sample is, then, provided directly to demodulators **650a** and **650b** and is delayed by one PN chip interval by delay elements **620** and **622** before being provided to demodulators **650c** and **650d**, respectively. The sample is PN descrambled in PN descrambling elements **654a**, **654b**, **654c** and **654d**. In the exemplary embodiment, PN descrambling elements **654a**, **654b**, **654c** and **654d** descramble the sample in accordance with two PN sequences (PN_I and PN_Q) provided by PN generator **[[656]] 606**. The complex descrambling operation is performed as described above with respect to complex despreading element **[[150a]] 150**.

[00157] The samples are provided at twice the PN chip rate. The samples are provided directly to demodulator **700a** and are delayed by one PN chip prior to being provided to demodulator **700b**. The sample is PN descrambled in PN descrambling elements **704a** and **704b**. In the exemplary embodiment, PN descrambling elements **704a** and **704b** descramble the sample in accordance with two PN sequences (PN_I and PN_Q) provided by PN generator **706**. The

complex descrambling operation is performed as described above with respect to complex despreading element **[[150a]] 150**.

[00166] The first sample is provided to sample combiners **[[834]] 834a-b** and is provided through switches **[[832]] 832a-b** to delay elements **[[828]] 828a-b**. Delay elements **[[828]] 828a-b** delay the sample by one half PN chip interval before providing the sample to a first summing input of summers **[[830]] 830a-b**. The second sample is then provided to equalizers **[[834]] 834a-b** and provided through switches **[[832]] 832a-b** to a second summing input of summer **[[830]] 830a-b**.

[00167] The two samples are summed together by summers **[[830]] 830a** and **830b** and the output is provided by sample combiner **834a** to demodulator **800a** and by sample ~~combiners **834b**~~ combiner **834b** to delay element **822**. Delay element **822** delays the result from summer **830b** by one PN chip interval before providing it to demodulator **800b**.

[00168] In demodulators **800a** and **800b,** the received summed samples are provided to PN descrambling elements **804a** and **804b**. In the exemplary embodiment, PN descrambling elements **804a** and **804b** descramble the sample in accordance with two PN sequences (PN_I and PN_Q) provided by PN generator **806**. The complex descrambling operation is performed as described above with respect to complex despreading element **[[150a]] 150**.